AMENDMENTS TO THE SPECIFICATION:

Please amend paragraph [0014] as follows:

[0014] Looking to the blocks in system 10, system 10 includes various items which in general are known in the prior art, but an additional scan feature as well as related control and operation distinguishes the overall system as detailed later. Looking by way of introduction to some of the blocks that are comparable to the prior art, they include a first-in first-out ("FIFO") memory 12 having a number *M* of word storage slots; by way of example, 256 such slots are shown and designated SL0 through SL255. However, the choice of 256 is only by way of illustration and one skilled in the art will recognize that the inventive teachings of this document may be implemented in different sized FIFO devices. In the preferred embodiment, each storage slot SL*x* has a same *N*-bit dimension, where that dimension may be any size. For the sake of example in this document, assume that this dimension is 8 bits, that is, each storage slot is operable to store an 8-bit word in eight respective data cells. Accordingly, in Figure 1, the eight bit positions are indicated as bit positions 0 through 7. Also included in system 10 are a write pointer PTR_{WT} and a read pointer PTR_{RD}. In general, write pointer PTR_{WT} indicates the word slot into which a next word will be written into FIFO memory 12. Conversely, read pointer PTR_{RD} indicates the word slot from which a next word will be read from FIFO memory 12. The implementation of, and indication by , the respective word pointers PTR_{WT} and PTR_{RD} may be achieved in various fashions ascertainable by one skilled in the art and consistent with the functionality described in this document. System 10 also includes a data read/write circuit 14 connected to FIFO memory 12 in a manner that allows a word to be written into, or read from, FIFO memory 12 in a given cycle, according to the indication of the relevant one of write pointer PTR_{WT} and read pointer PTR_{RD}. In one mode, read/write circuit 14 is operable to communicate data[[e]] with respect to the system data path, and

for testing it may communicate elsewhere as further detailed below. Also, data read/write circuit 14 may be constructed in various manners, such as to include multiplexing circuitry or the like.

Please amend paragraph [0021] as follows:

[0021] In step 40, method 30 determines whether all scan words have been written into, and read from, FIFO memory 12. In other words, some determined number of scan words will be known as to be used for testing FIFO memory 12, and step 40 will therefore determine whether each of these words has been input and output with respect to FIFO memory 12 for testing. In a contemporary application, the number of total tested words may vary based on various considerations. In an ideal case, only a single write/read cycle would be needed to test the correct behavior of a given word; however, due to aliasing and other effects, there is a need for ~~much~~ more cycles to exhaustively test memory 12 array with various sequences. These sequences are known as "march patterns" and they consist in writing/reading various values in words at various locations with a defined order. A common way to name those algorithms is by the number of cycles it requires per word, say "*LM*". For example, a "13*M*" algorithm requires a given word to be accessed 13 times and thus the complete memory will require 13*M* accesses to be fully tested. There are actually several embedded cycle loops involved in testing the full memory structure, including: (1) the *N* loop to input/output one scan slot18; (2) the *M* loop repeating *M* times the *N* loop to shift in/out the complete arrays contents one time; and (3) the *L* loop repeating *L* times the *M* loop to insure the array is exhaustively tested as per the "*LM*" algorithm. Thus, the total number of clock cycles to test the FIFO would thus be roughly *L*M*N* and the number of total tested words may be on the order of *L*M*, where typical values for *L* is 8 to 16. In any event, if step 40 determines that not all test words have been so processed, then

method 30 continues from step 40 to step 42, where both read pointer PTR_{RD} and write pointer PTR_{WT} are advanced. Thus, in the current example, where prior to reaching step 42 those pointers both point to slot SL0, then in the first instance of step 42 each of those pointers advances to slot SL1. Note also that in a later instance of step 42 and once the pointers are pointing to the logical top of FIFO memory 12 (i.e., slot SL255), then the step 42 advancement of those pointers causes them to wrap around to the logical bottom of FIFO memory 12 such that they again then point to slot SL0. Returning to step 40, if it determines that all test words have been input and output, then method 30 continues from step 40 to step 44. Step 44 is a capture cycle, which is used in the same general sense as the prior art, namely, the sequence of test data words that has been read from FIFO memory 12 is analyzed to determine whether it departs in any way from that which is expected. Any such departure leads to an investigation and identification of the location in FIFO memory 12 that produced the erroneous data, thereby indicating a possible faulty storage element(s) in FIFO memory 12. If a fault is detected, corrective action may then be taken if possible or the problematic device may be separated from usable inventory.